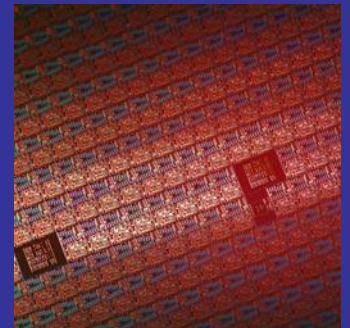# Material- and polishing-induced defectivity on EUV mask substrates

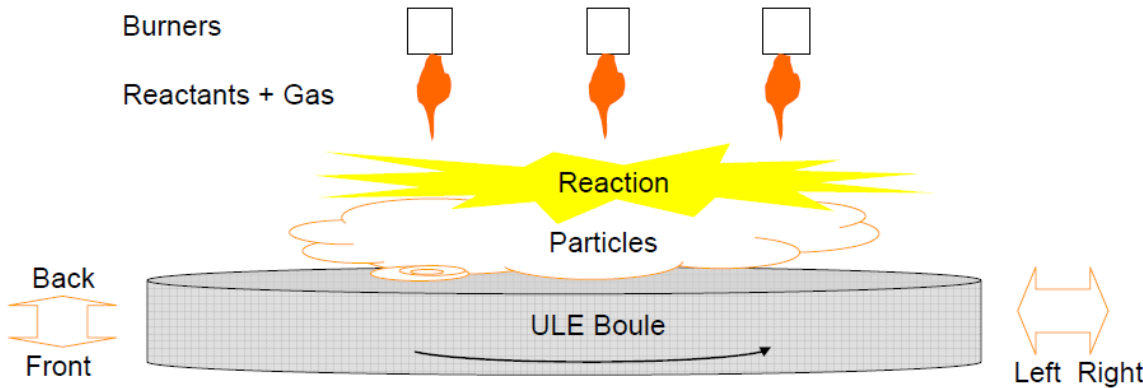R. Teki*, A. John-Kadaksham, A. Ma, F. Goodwin
SEMATECH, Albany, USA

T. Yatsui, M. Ohtsu
Nanophotonics Research Center, Tokyo, Japan

A. Hariprasad, U. R. K. Lagudu, S. V. Babu
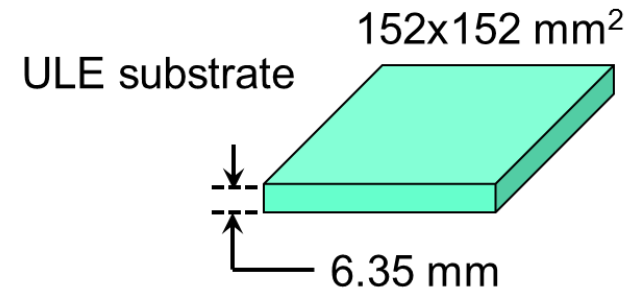Clarkson University, Potsdam, USA

P. Dumas, R. Jenkins
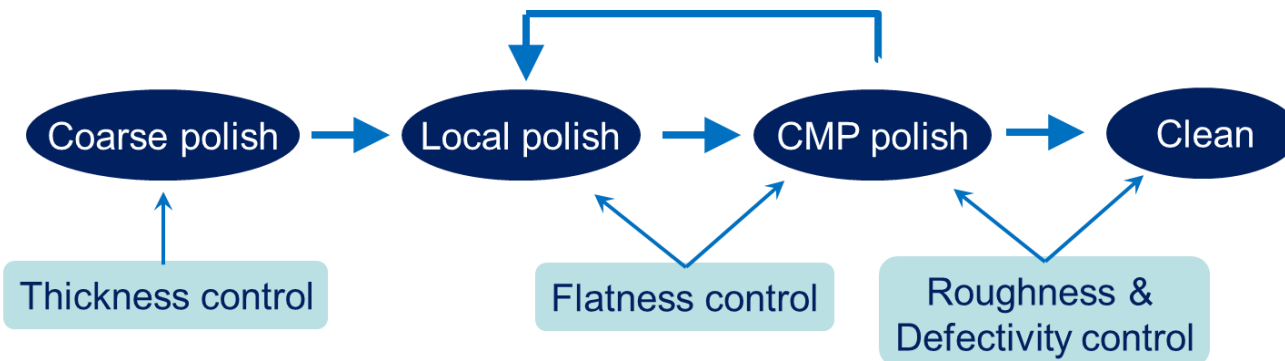QED Technologies, Rochester, USA

Substrate processing

Flame hydrolysis process for TiO_2-doped fused silica

152x152 mm²

ULE substrate

6.35 mm

Substrate dimensions

Thickness control

Flatness control

Roughness & Defectivity control

Substrates undergo iterative global/local polishing techniques

Defectivity

0.03 /cm²

30 nm P-V

Flatness

0.05 nm RMS
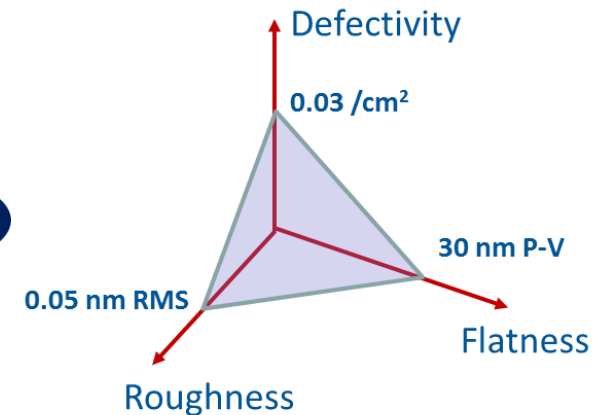
Roughness

Substrate specifications

Substrate trends

RMS Roughness (nm) for CMP @ Clarkson
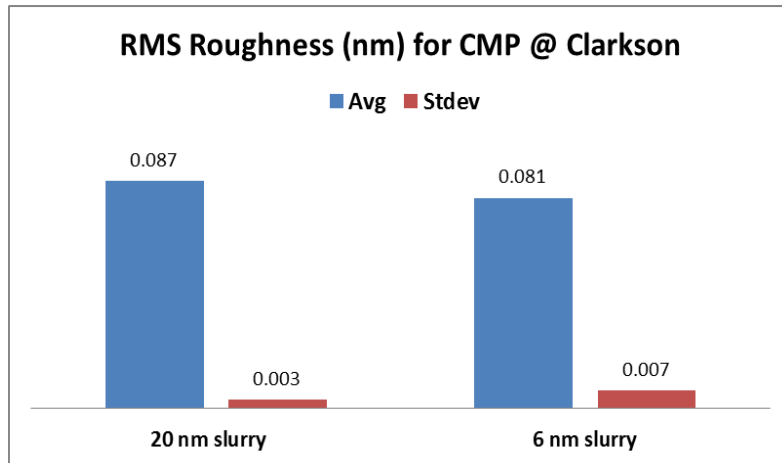
Roughness specification is easy to achieve but defectivity is very hard
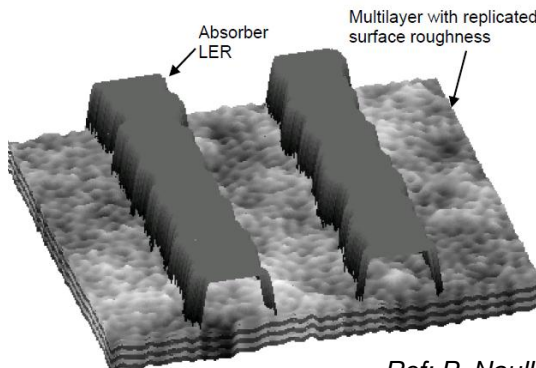

Platinum

Fused silica

5 nm
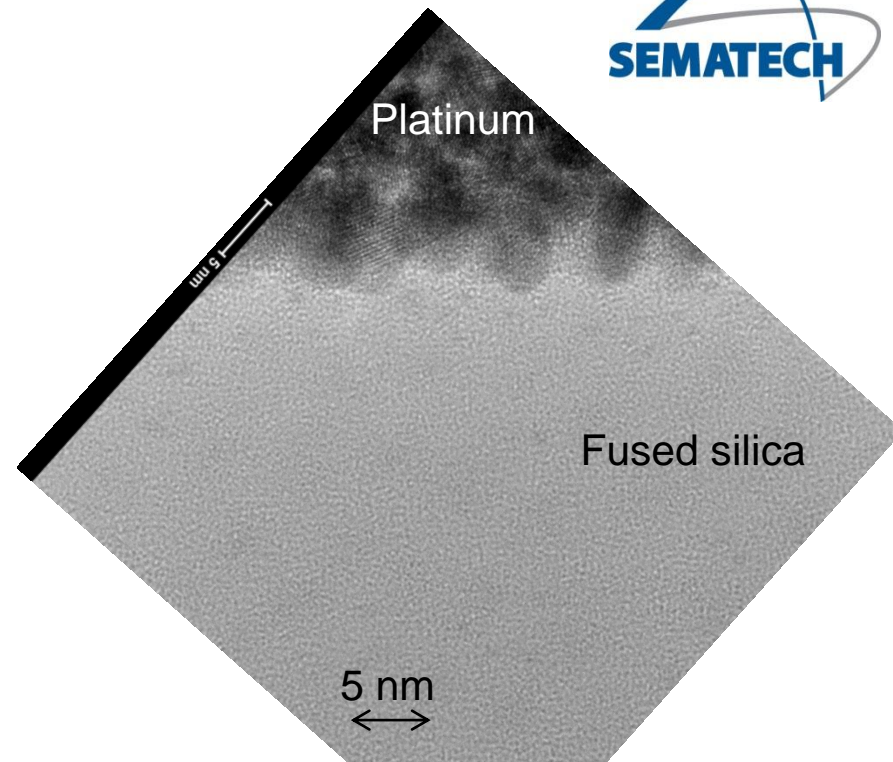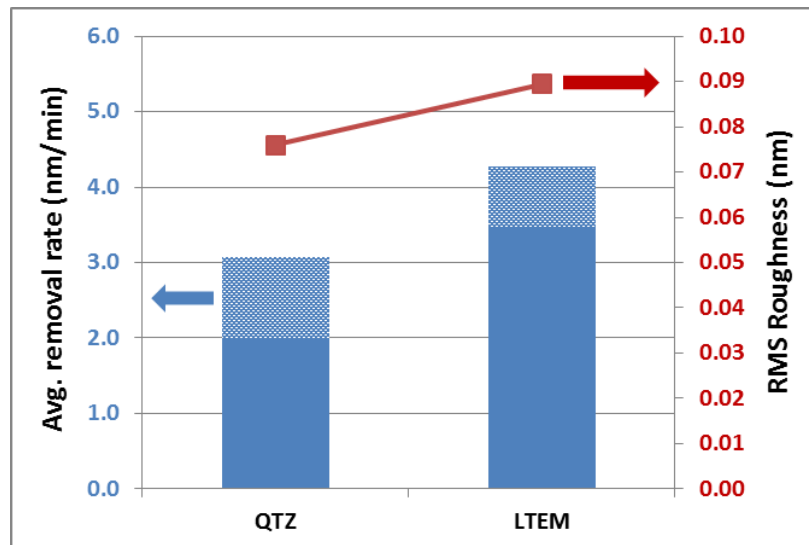
No indication of sub-surface damage at the top surface of supplier substrate in a HR-TEM micrograph

- LTEM & QZ for same CMP conditions:
  - LTEM has a higher removal rate than QZ
  - LTEM has greater roughness than QZ
  - LTEM has more pits/scratches than QZ

Effect of roughness on defectivity, inspection sensitivity & LER
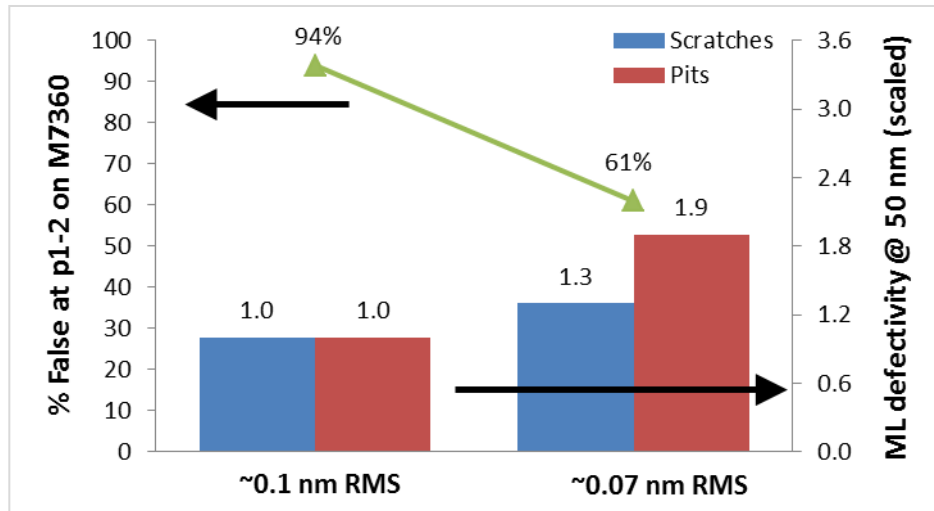
Lower roughness substrates show better capture efficiency but higher defectivity (more polishing)

	Depth	SEVD	FWHM
P1	1.9	31.5	73.4
P1	3.3	29.5	48.7

At lower roughness, the M7360 is able to pick up shallower and wider pit defects

The phase roughness may or may not affect LER – current requirement range is between 0.05 - 0.3 nm.

Ref: P. Naulleau et. al., SPIE EUV Litho. 2010, A. Vaglio Pret et. al., EUVL 2012

Overview of SPIE 2012


```
                        ┌─────────────────────┐
                        │  Smoothing options  │
                        └─────────────────────┘
              ┌──────────────────┼──────────────────┐
     ┌────────────────┐  ┌────────────────┐  ┌────────────────┐
     │ Substrate-based│  │  Silicon-based │  │  Coating-based │
     └────────────────┘  └────────────────┘  └────────────────┘
```
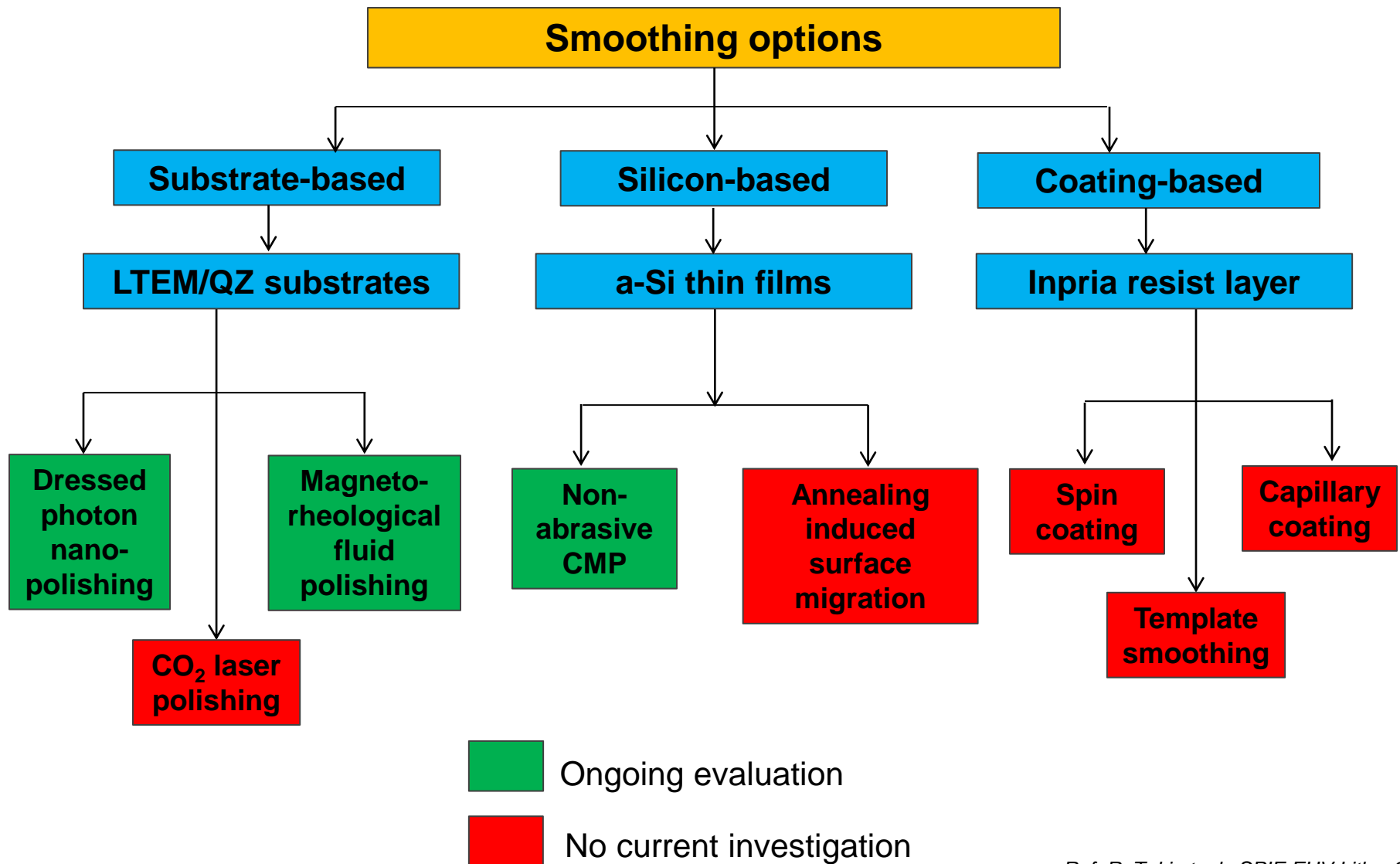
Substrate-based	Silicon-based	Coating-based
LTEM/QZ substrates	a-Si thin films	Inpria resist layer

Dressed photon nano-polishing

Magneto-rheological fluid polishing

CO_2 laser polishing

Non-abrasive CMP

Annealing induced surface migration

Spin coating

Capillary coating

Template smoothing

Ongoing evaluation

No current investigation

Magneto-rheological finishing

- Principle:
  - MR fluid properties (e.g., viscosity) change in milliseconds with magnetic field
  - No fluid wear - repeatable, precise and deterministic
  - Removal based on shear forces – less potential for sub-surface damage
  - Shown to achieve flatness < 30 nm P-V over 142x142 mm^2 area on LTEM substrates
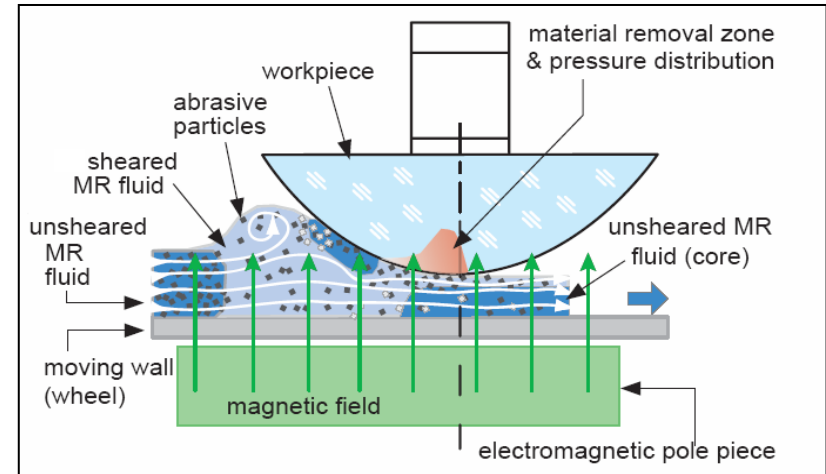
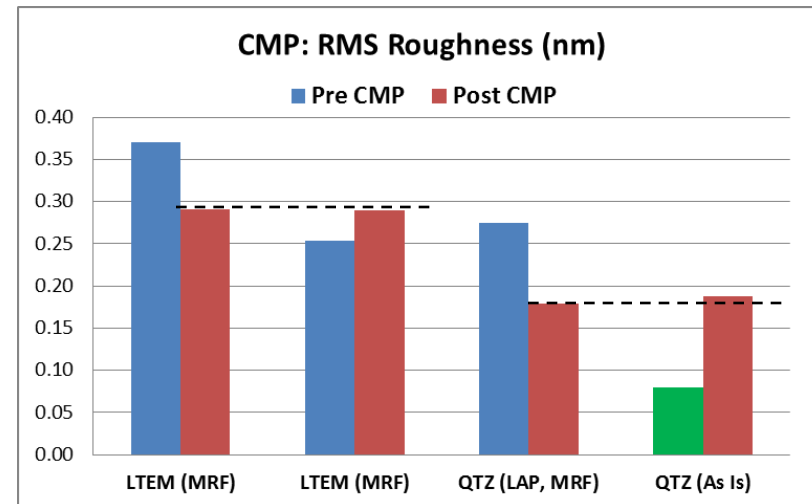MRF: P-V Flatness (nm) over 142x142 mm^2
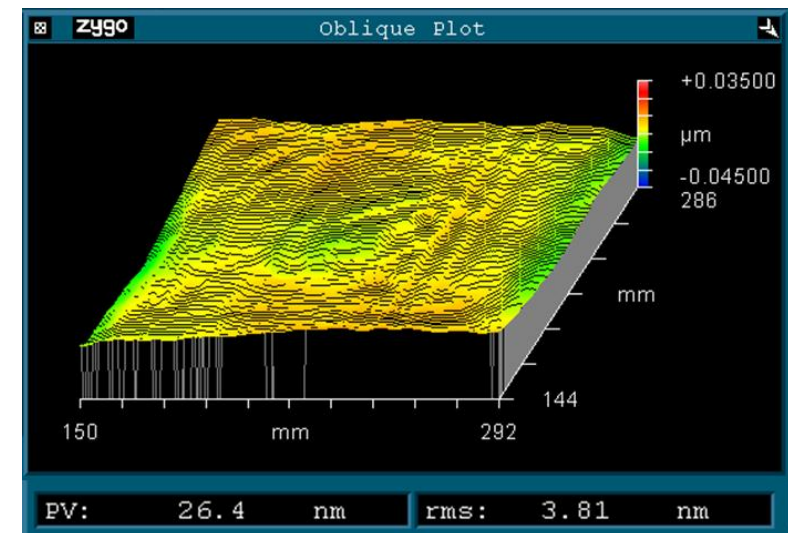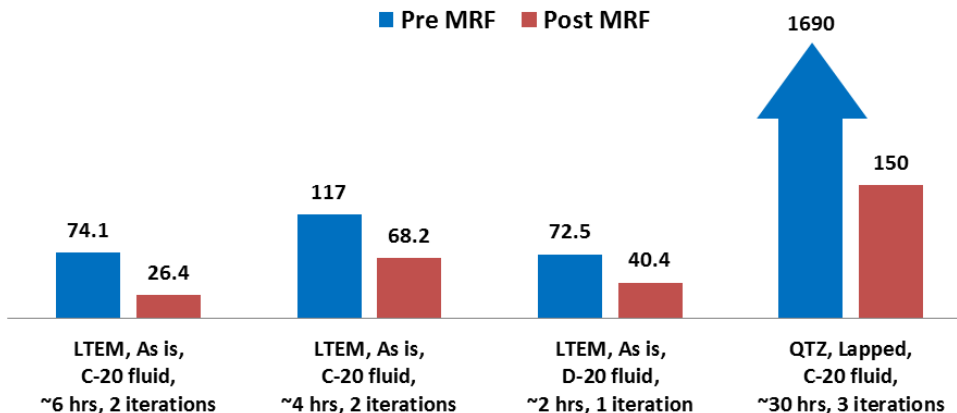
MRF followed by CMP
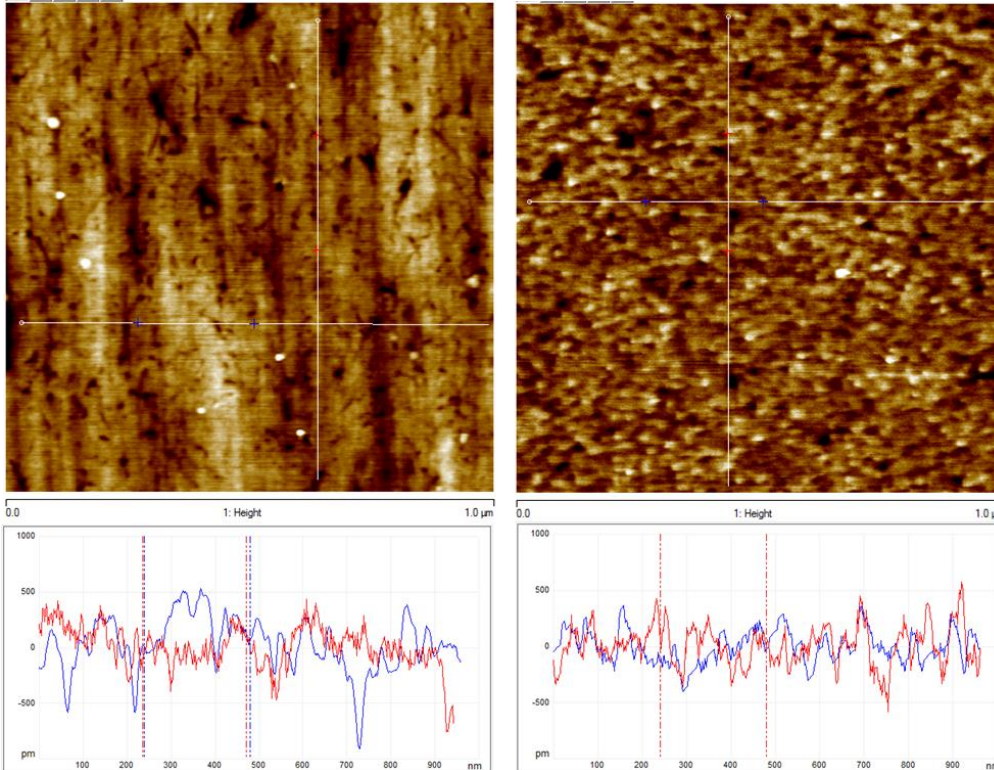
CMP is able to remove the signature unidirectional grooves produced by MRF polishing

CMP results in similar surface roughness irrespective of whether MRF polished or not (LTEM > QZ)
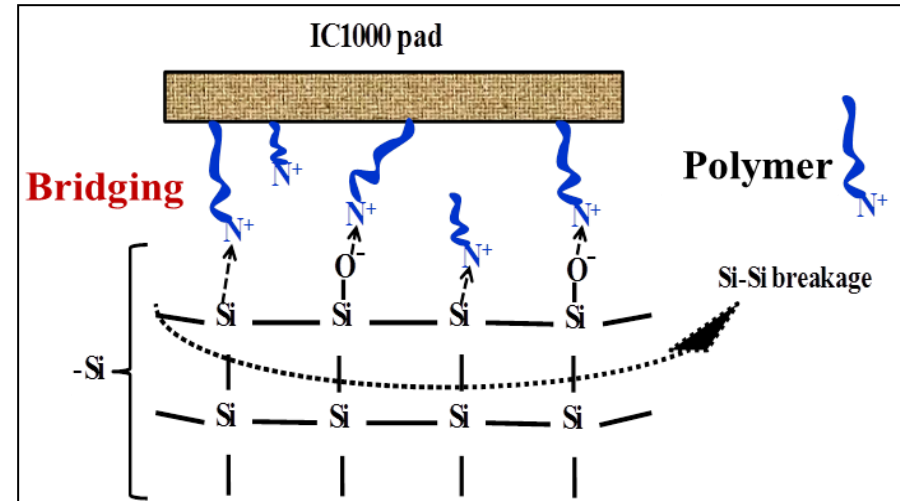

Next step(s): evaluate effect on defectivity and estimate CMP-induced flatness degradation
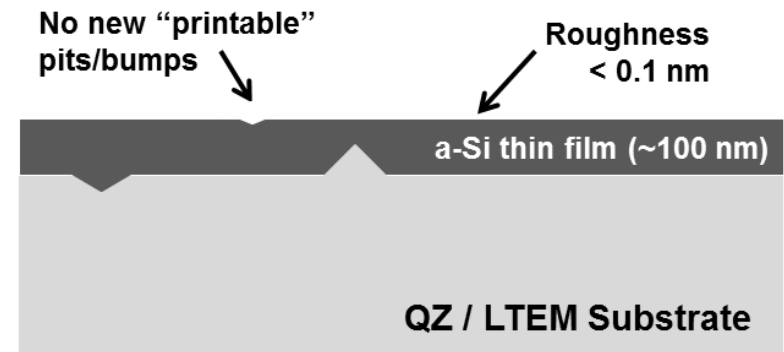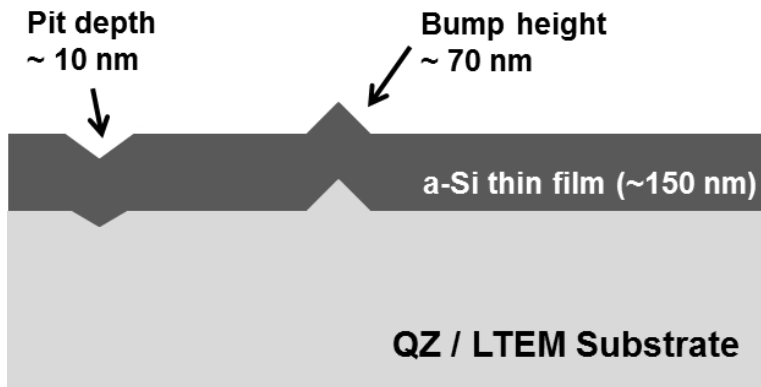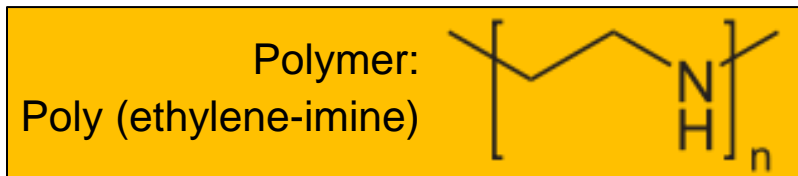
Non-abrasive a-Si CMP

- Principle:
  - Pits/scratches are largely caused by abrasive slurry particles
  - Deposit a-Si thin film and perform CMP without using slurry particles
  - Removal is based on differing energies of the bonds formed by the polymer with the polishing pad and the substrate surface

Polymer:
Poly (ethylene-imine)

Courtesy: Prof. S. V. Babu, Clarkson University

$$E(-Si-Si-) < E(Bridging) < E(-Si-O-\ \&\ -Si-N-)$$

Pit depth ~ 10 nm
Bump height ~ 70 nm

a-Si thin film (~150 nm)

QZ / LTEM Substrate

No new "printable" pits/bumps
Roughness < 0.1 nm

a-Si thin film (~100 nm)

QZ / LTEM Substrate

Non-abrasive a-Si CMP

- Advantages:
  - No new tools required (deposit a-Si film in the same Ion-beam deposition tool)
  - CMP by its nature may add >0 defects, but can potentially increase yield of lower defectivity substrates
  - Cheaper process development, since this applies to both LTEM & QZ substrates
  - Cleaning will be similar to ML blank cleaning

a-Si RMS Roughness
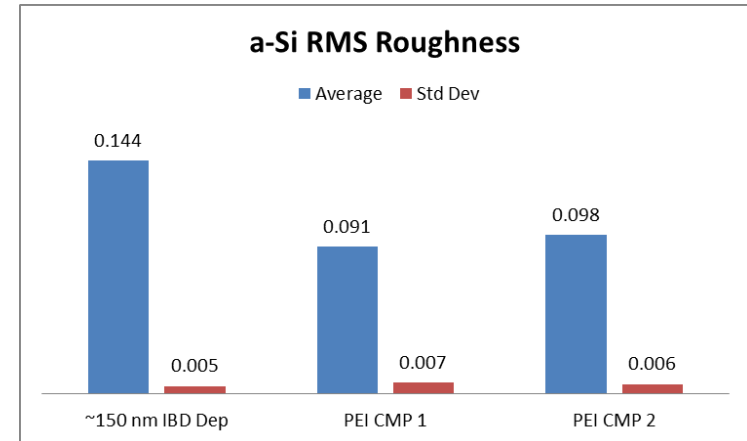
Sub-A roughness on a-Si coated substrates
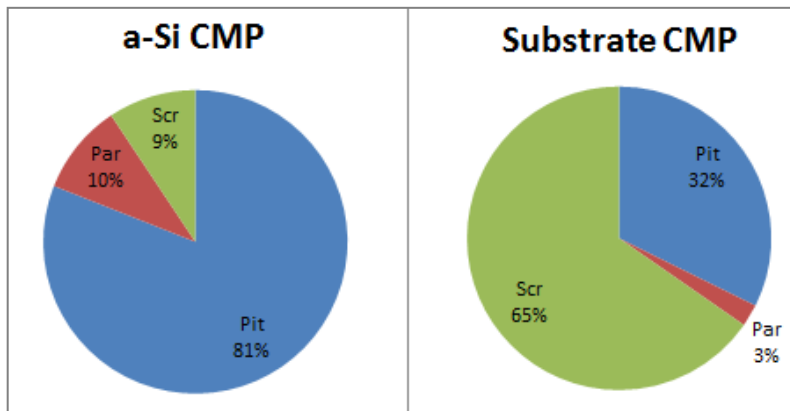
7x reduction in % scratches on same CMP tool

d = 3.2 nm

Complete smoothing of a pit
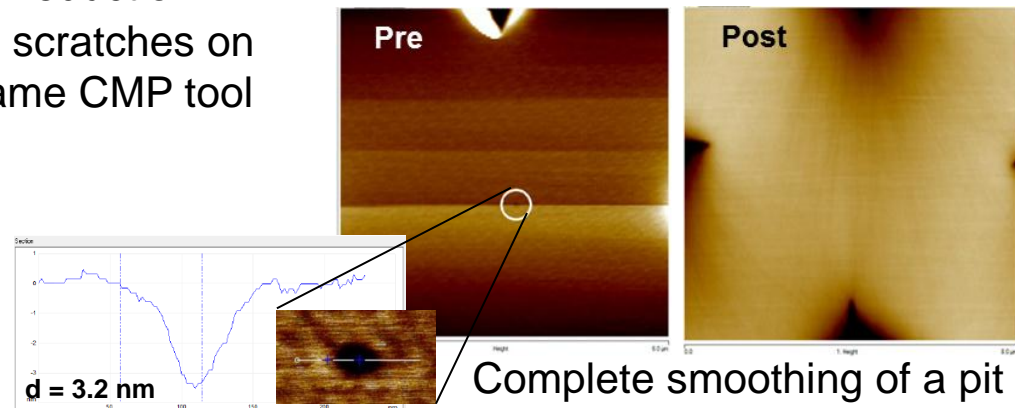
Next step(s): Transfer process to clean tool and evaluate pit/scratch adders from a-Si CMP+Clean

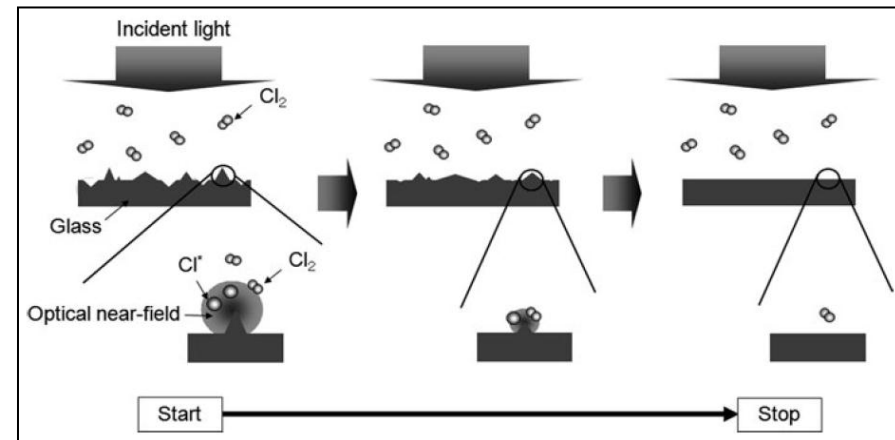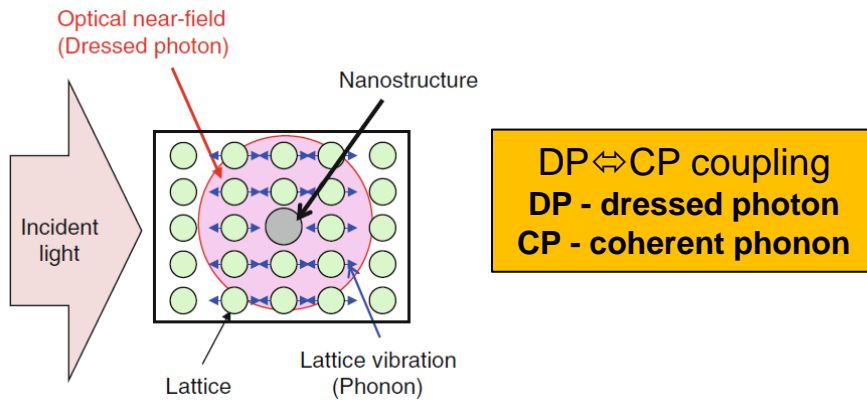# Dressed-photon nanopolishing

Optical near-field (Dressed photon)

Nanostructure

Incident light

Lattice

Lattice vibration (Phonon)

DP⇔CP coupling
DP - dressed photon
CP - coherent phonon

Ref: M. Ohtsu (ed.), Progress in Nanophotonics
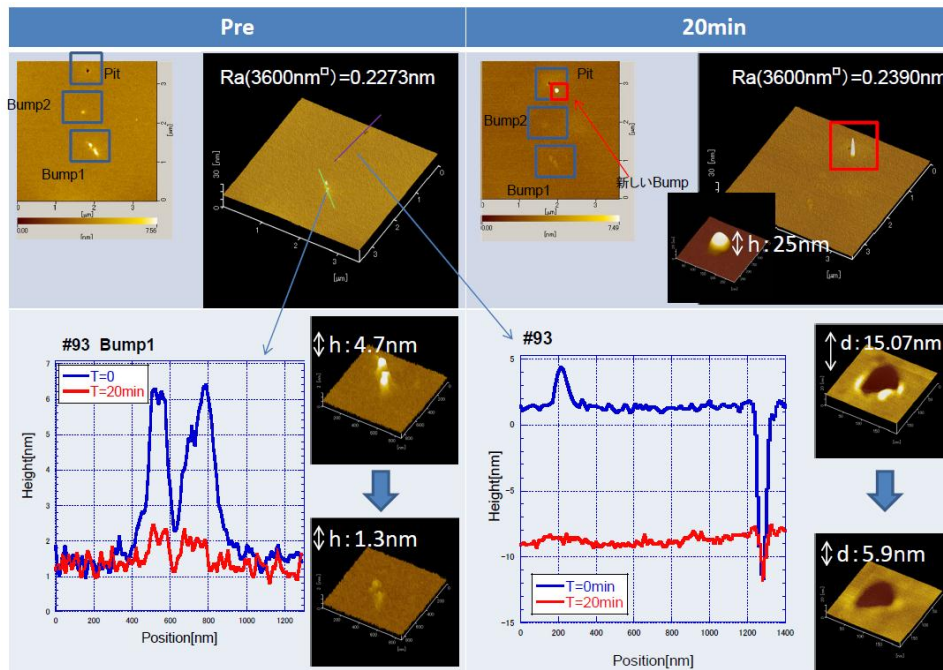
- Principle:
  - DP-CPs are generated at surface tips and exchanged between Cl_2 molecules to enable dissociation and localized etching
  - Etching stops when surface becomes flat so that DP-CPs are no longer generated
  - No etching occurs above flat surfaces
  - Shown to simultaneously smooth both pit and particle defects (to below 1 nm), while not increasing surface roughness

DPNP process adders
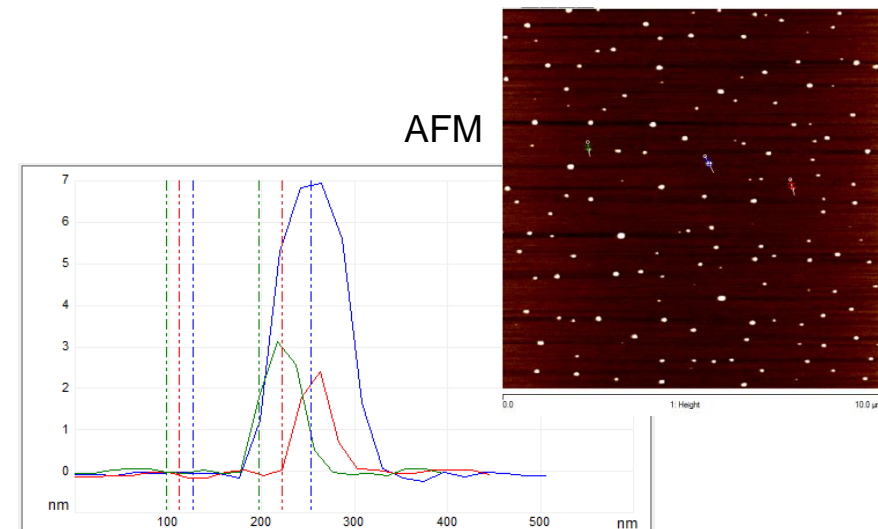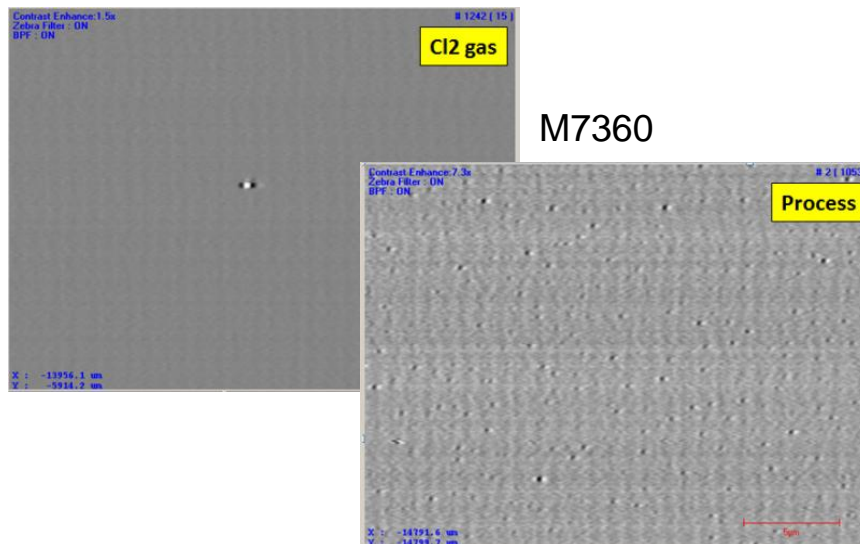
Pre DPNP, M7360

~10

Post DPNP, M1350

~100000

Post DPNP-clean, M7360

~100

Aprox. DPNP spot location (30 min)
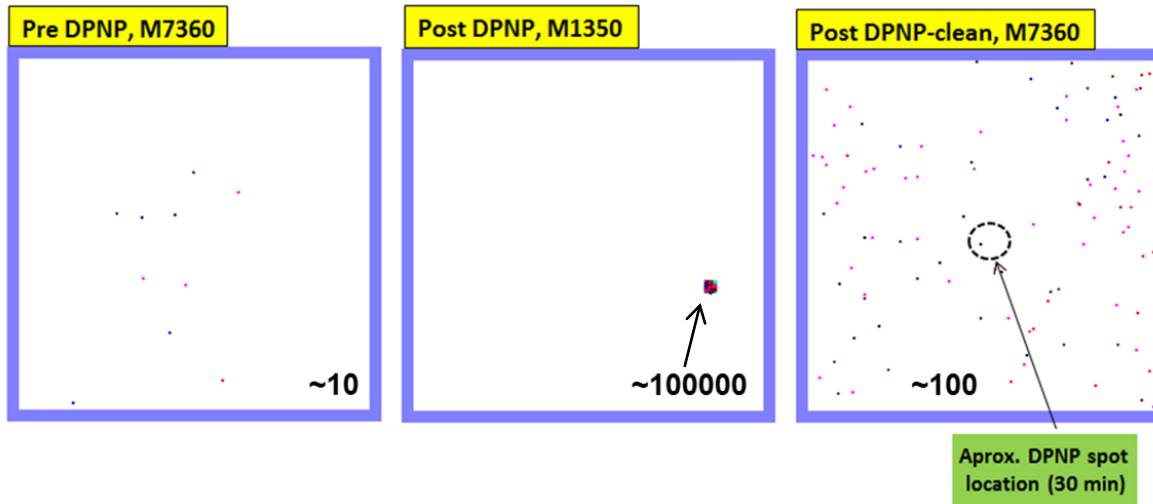
– The combination of etchant gas and laser exposure seems to be adding many small (2-7 nm high) bumps

– These are most likely chemical residues; standard cleaning was effective in removing all of them (cleaning needs optimization).
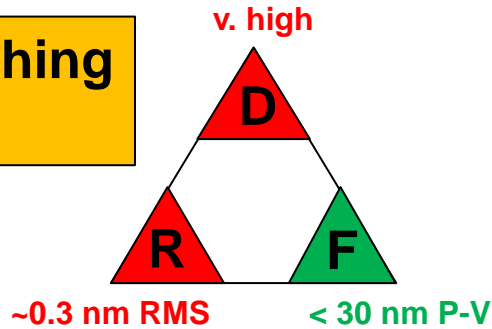
Cl2 gas

M7360

Process

AFM

Next step(s): look into mechanism of pit etching and enlarge the exposed laser beam spot

Effect on specifications

Local polishing (MRF)

- leaves grooves
- higher roughness

v. high

D (red)

R (red) ~0.3 nm RMS   F (green) < 30 nm P-V

Global polishing (CMP)

- add particles to polish
- need to remove them
- substrate thickness

double digits

D (red)

R (green) < 0.07 nm RMS   F (red) degrades
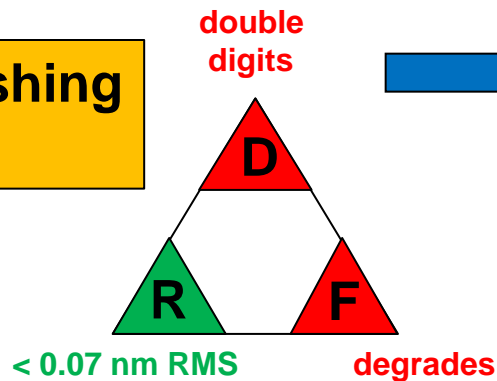
Cleaning (Chemicals/MHz)

- removes most particles
- can add pits
- can increase roughness

single digit

D (green)

R (red) might increase   F (green) no effect

Defect smoothing (DPNP)

- non-contact
- for pits, embedded particles

0 (?)

D (green)

R (green) < 0.07 nm RMS   F (green) no effect (need to confirm)
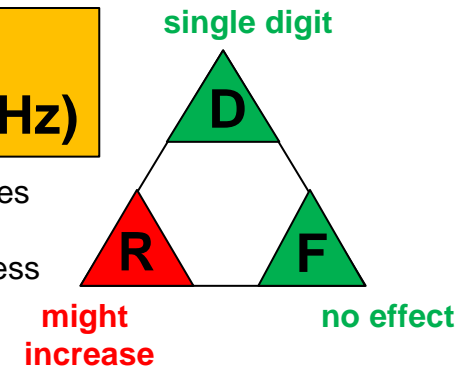
What we need

1. Need tightly integrated substrate polishing process development to simultaneously meet the three <u>coupled</u> requirements of flatness, roughness and defectivity.

2. Need higher inspection sensitivity (better tools, lower roughness) to detect substrate defects before ML deposition. Only 10% yield on quality deposited ML blanks.

3. Need to confirm what roughness levels - with regards to LER - are acceptable for production at 22 nm & future nodes.
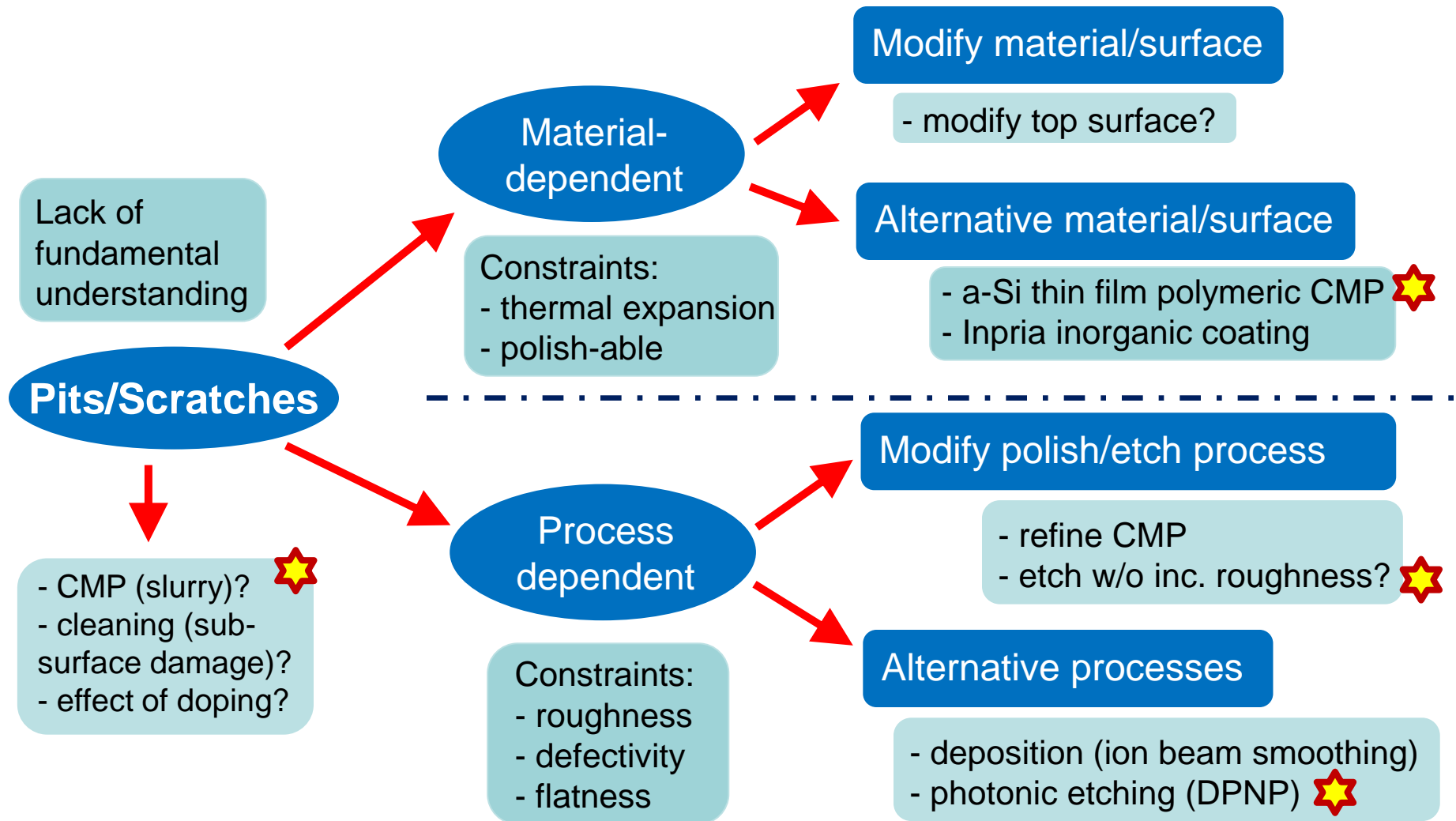
4. Need to determine the size/shape of defects that are printable and if they can be detected at the current roughness levels. If we don't detect every printable defect, we can't verify it on AIMS tool and repair using any of the current techniques.

Addressing substrate issues

Lack of fundamental understanding

Pits/Scratches

- CMP (slurry)?
- cleaning (sub-surface damage)?
- effect of doping?

Material-dependent

Constraints:
- thermal expansion
- polish-able

Modify material/surface

- modify top surface?

Alternative material/surface

- a-Si thin film polymeric CMP ⭐
- Inpria inorganic coating

Process dependent

Constraints:
- roughness
- defectivity
- flatness

Modify polish/etch process

- refine CMP
- etch w/o inc. roughness? ⭐

Alternative processes

- deposition (ion beam smoothing)
- photonic etching (DPNP) ⭐

⭐ Currently working on